REMARKS/ARGUMENTS

Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art (AAPA) in view of Weldon et al. (US 6,956,922, hereafter referred to as "Weldon").

Response:

Independent claims 1 and 5 have been amended to overcome these claim rejections. Claims 1 and 5 now recite that the logic unit controls the frequency divider to generate the character clock by dividing the number of cycles of the pixel clock during part of the predetermined interval by a first number. Division by the first number produces a quotient and a remainder, with the remainder being equal to a second number of remaining clock pixels. By definition of the remainder, the second number is less than the first number.

The logic unit adds one or more extra cycles of the pixel clock to cycles of the character clock during the predetermined interval until the second number of remaining pixel clocks have all been added to cycles of the character clock. In this way, there is no fractional character clock periods produced by the frequency divider since all of the remaining pixel clock cycles are added to existing character clock cycles. In addition, claim 1 has been amended to specify that the logic unit is directly connected to the frequency divider. The claim amendments are fully supported in Figures 5-7 and paragraphs 19-22 of the instant application, and no new matter is added.

The AAPA does not teach that the logic unit is directly connected to the frequency divider, as is recited in the currently amended claim 1.

Weldon teaches a way to divide a clock frequency by a non-integer amount,

such as 4.5. In order to accomplish this, the non-integer clock divider 130 shown in Figures 1 and 2 will alternatively count to integers K and K+1, such as 4 and 5. By logically combining the divided clock periods produced by counting to K and K+1, the non-integer clock divider 130 produces a clock period having a non-integer value of K+1/2, such as 4.5.

In Weldon's teaching, the first divisor K and the second divisor K+1 are always related to each other, and always have a difference of 1. In addition, the non-integer clock divider 130 must always alternatively divide the input clock signal by K and then by K+1. Therefore, Weldon's clock divider is not as flexible as the claimed invention's clock divider, which is not limited to dividing only by a factor of K+1/2.

Weldon does not teach dividing the number of cycles of the pixel clock during part of the predetermined interval by a first number for producing a quotient and a remainder equal to a second number of remaining clock pixels. Weldon also does not teach the logic unit adding one or more extra cycles of the pixel clock to cycles of the character clock during the predetermined interval until the second number of remaining pixel clocks have all been added to cycles of the character clock. Moreover, Weldon does not teach that the second number is less than the first number. For these reasons, the applicant submits that independent claims 1 and 5 are patentable over the combination of the AAPA and Weldon.

Claims 2 and 6 have also been amended to distinguish from the cited prior art. Each of these claims recites that durations of both high and low states of the character clock are multiples of the pixel clock period. This amendment is fully supported in Figure 5 and paragraphs 20 and 21 of the instant application, and no new matter is added. As shown in Figure 5, the high states of the character clock have durations that are 4 times the period of the pixel clock. The low states of the

character clock have durations that are 4 times, or occasionally 10 times, the period of the pixel clock.

On the other hand, Weldon teaches in Figure 3 that the high states of the output clock have a duration of two times the period of the clock signal, but the low states of the output clock have a duration of 2.5 times the period of the clock signal. Therefore, Weldon does not teach the limitations of amended claims 2 and 6.

Furthermore, claims 2, 3, 6, and 7 are dependent on claims 1 and 5, and should be allowed if their respective base claims are allowed. Reconsideration of claims 1-3 and 5-7 is therefore respectfully requested.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Sincerely yours,

/Winston Hsu/ Date: 01.11.2007

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